

2024

# CHIPLETS SOLUTIONS FOR CUSTOM IC *Design Workshop*



*April 25th, 2024 – Denver, CO – USA*

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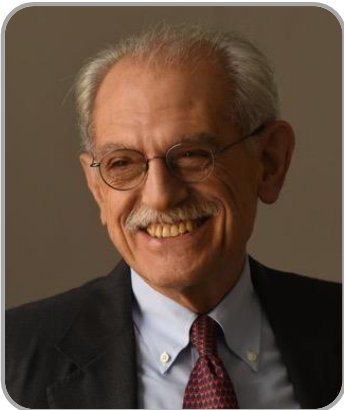


## Program

# Alberto Sangiovanni-Vincentelli

*University of California, Berkeley*

KEYNOTE: Chiplet-based electronics: evolution or revolution?



**Abstract:** Chiplets are seen as a strategic option to overcome the slowing down of the Moore's law and to optimize integrated circuit design going beyond the physical boundaries of a single chip. Several examples of effective system design using chiplets and advanced packaging solutions have been reported in industry. These designs offer great opportunities but also challenges for methodologies and tools. Adding the multi-chip option, increases significantly the design space and new partitioning and evaluation tools have to be developed. The EDA industry is already offering partially integrated solutions for designers but more needs to be done to offer a seamless environment. Is then chiplet-based design a revolution in the way we think of integrated system design? Multi-chip modules attracted the attention of industry and academia in the 1980s and even earlier. However, the several startups that were born in that time frame went down without significant legacy. Is chiplet-based design an incremental innovation versus

the multi-chip modules? Which opportunities are now compelling versus the past? Will chiplet-based design generate new companies specialized in this technology that will offer technology services similar to the ones we see for foundries? What will be the role of the EDA industry in facilitating the ecosystem?

**Bio:** Alberto Sangiovanni-Vincentelli joined the Department of Electrical Engineering and Computer Sciences University of California, Berkeley in 1976 where he holds the Edgar L. and Harold H. Buttner Chair. He co-founded Cadence and Synopsys, the two largest companies in the EDA industry. Sangiovanni-Vincentelli's influence extends beyond academia and business, as evidenced by his advisory roles to global technology companies and governmental bodies, including IBM, Intel, United Technologies, BMW, General Motors, and Pirelli. He has also been actively involved in various educational and governmental advisory capacities. His scholarly contributions are substantial, with over 1000 papers and seventeen books focusing on design tools, methodologies, large-scale systems, embedded controllers, and hybrid systems. Recognized as an IEEE Fellow since 1982, an ACM Fellow and a member of the National Academy of Engineering since 1998, he has received numerous awards, including the IEEE/RSE Maxwell Medal “for groundbreaking contributions that have had an exceptional impact on the development of electronics and electrical engineering or related fields” and the BBVA Frontiers of Knowledge Award in the Information and Communication Technologies category with the following motivation: “for transforming chip design from a handcrafted process to the automated industry that power today’s electronic devices”. Currently, he serves on the Board of Directors of Cadence Design Systems Inc., and nine USA, India, and European companies, of which he is Chairman of the Board on five, and continues his academic role at UC Berkeley.

## Eric Fetzer

*Intel*

### Advanced Technologies For Next Generation Chiplet Based Data Center CPU



**Abstract:** The datacenter CPU can benefit greatly from advanced heterogeneous integration technologies to achieve optimized performance and cost. This presentation highlights advances in logic and packaging technologies that can deliver optimized ultra-high-density compute in the most power-efficient manner, as exemplified in Intel’s second generation Efficiency core based Xeon datacenter CPU (Clearwater Forest). Several advanced logic and heterogeneous integration technologies have been leveraged to achieve an optimized data center dense compute with leading edge energy-efficiency, optimally integrating I/O die tiles, fabric and memory base dies, and compute chiplets . The presentation will discuss this pioneering approach to high-performance throughput server computing architecture, and present how Intel envisions these component technologies to become critical building blocks for future silicon-based computing systems with the intent to make these

technologies available to Intel foundry customers. These new chiplet enabling technology components include: 1. RibbonFET – the latest advancement in transistor architecture on intel’s 18A process technology; 2. PowerVIA – the latest advancement in power delivery technology being introduced on Intel’s 18A process technology; 3. Foveros Direct – Hybrid bonding technology to enable high-density direct stacking of active chips; 4. EMIB – Second generation embedded integrated bridge (EMIB) technology; 5. A combination of 3 logic process technologies (Intel 7, Intel 3, Intel 18A) in one package enabling a cost effective and power efficient approach to delivering an ultra-dense package level transistor count. Intel’s next generation Clearwater Forest Xeon datacenter server CPU exemplifies optimal use of these advanced chiplet integration technologies and provides a use case example for how Intel customers can leverage the same advanced chiplet technologies for their own products.

**Bio:** Eric S. Fetzer is an Intel Fellow in charge of Technology Alignment and Pathfinding in the Design Engineering Group. Eric is responsible for product process co-optimization and pathfinding solutions at the intersection of design, silicon process, advanced packaging, architecture, and test. Prior to assuming his current role, Fetzer led design convergence efforts on Intel Atom Microservers, and drove circuit design methodology Intel Xeon Processors. Earlier in his Intel career, he was responsible for various aspects of the design including array design, clock distribution, timing convergence, power delivery, and silicon debug of Intel Xeon and Intel® Itanium® processors. Before joining Intel in 2005, Eric held design engineering positions at Hewlett Packard Enterprise, and IBM. Fetzer earned a bachelor's degree in electrical and computer engineering from the University of Wisconsin – Madison in 1996. His work in the areas of circuit design, memories, SOC clocking, and power management has led to sixteen U.S. patents and over a dozen peer reviewed publications.

## Zhengya Zhang

*University of Michigan, Ann Arbor*

### Harnessing Chipllets for Academic Research



**Abstract:** The development of monolithic chips to match ever-evolving computing workloads is both expensive and challenging. Alternatively, modular chipllets can be designed and reused to create multi-chip packages (MCPs) capable of addressing diverse workloads. In this presentation, I will share two MCPs resulting from our collaboration with Intel and the Institute of Microelectronics in Singapore. The first MCP, Arvon, utilizes Embedded Multi-die Interconnect Bridge (EMIB) to integrate an FPGA chipllet and a DSP chipllet. The second MCP, NetFlex, integrates four neural network chipllets using high-density fan-out wafer level packaging (HD-FOWLP). Our experience demonstrates the potential of leveraging chipllets and MCPs in academic research, while also recognizing the challenges that need to be addressed for this approach to thrive.

**Bio:** Zhengya Zhang received the B.A.Sc. degree from the University of Waterloo in 2003, and the M.S. and Ph.D. degrees from UC Berkeley in 2005 and 2009, respectively. Since 2009, he has been with the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, where he is currently a professor. His research primarily focuses on low-power and high-performance VLSI circuits and systems, with applications in computing, communications, and signal processing. Dr. Zhang was a recipient of the NSF CAREER Award, the Intel Early Career Faculty Award, the Neil Van Eenam Memorial Award from the University of Michigan, and the David J. Sakrison Memorial Prize from UC Berkeley. He serves as an IEEE Solid-State Circuits Society Distinguished Lecturer.

# Jason Rupe

*Cable Labs*

## Chiplet Reliability and Reliable Use of Chiplet Technology



**Abstract:** Integrated Circuit (IC) reliability is well understood, and an advantage to IC use. With the advent of Chiplets, which dis-integrates IC functions into more general parts, IC packaging becomes the new reliability challenge. While there is relevant research being conducted on this problem space, there are other challenges brought by Chiplets which also bring challenges to reliable Chiplet packaging into systems. But that is only part of the story: some of the advantages of Chiplets can bring new reliability advantages at the system level, and many of these advantages translate to larger concepts of reliability. In some use cases, these higher concepts of reliability matter more, and lead to further interest in Chiplets for some applications.

**Bio:** Jason got his Ph.D. modeling large scale systems and networks for performance and reliability from Texas A&M. He has held titles including senior technical staff and director at USWEST, Qwest, Polar Star Consulting, and Tenica. He was the last Managing Editor for the IEEE Transactions on Reliability, Denver Section Chair, and co-chair of IEEE Blockchain initiative. He is currently the Treasurer for the IEEE Reliability Society and supports failedb.io and other initiatives. At CableLabs, he is the Distinguished Technologist working on Proactive Network Maintenance, Network and Service Reliability, DOCSIS® Tools and Readiness, optical operations and maintenance, and reliability advancement for the industry. He was the RS Engineer of the year for 2021, and CableLabs inventor of the year for 2020.

# Shan Gao

*TSMC*

## Chiplet and Heterogeneous Integration with Advanced Packaging Technologies



**Abstract:** AI Large Language Model (LLM) training or inferencing applications always require huge amounts of data processing and communication in real time, which drives high performance computing and high bandwidth network product development. Due to the slowing down of Moore's law, chiplets and heterogeneous integration (HI) emerge as two key technologies to extend Si transistor scaling and PPAC optimization (performance, power, area, cost). HI allows for greater flexibility in the design of chiplets and products could be designed with chiplets of different sizes, different Si technologies, different functions (logic, memory, photonics, etc), and from different foundries, to be integrated into a single complex product/system. The paper focuses on the design, process, material, and reliability aspects of chiplet and heterogeneous integration with advanced packaging technologies. Various TSMC 3DFabric technologies, such as 2.5D CoWoS, 3D SoIC, System on Wafer (SoW) and Si Photonics package technologies, and their development directions/trends are presented. The business

and collaboration models between design house, EDA, foundries, packaging house to enable HI are described. The challenges to enable HI such as chip partitioning/splitting design, 2.5D/3D integration with TSV, testing, etc are also addressed.

**Bio:** Dr. Shan Gao is currently Director of Advanced Packaging Business Development at TSMC. He has over 20 years of experience in the microelectronics industry and is specialized in Semiconductor Interconnect & Advanced Packaging technologies, such as 3DIC, 2.5D CoWoS, FcBGA & CPI, etc. Prior to joining TSMC, he had served various advanced package technology development and product development positions at Hi-Silicon, Globalfoundries, Samsung, Institute of Microelectronics, etc. Dr. Gao holds a Ph.D degree in Materials Science from Technical University Munich, Germany.

# Dean Gonzales

*AMD*

## Scaling Chiplet IO Signal Integrity For The Next Generation Data Center



**Abstract:** Advanced packaging 3D Chiplet technologies have enabled dense heterogenous compute of soaring complexity, necessitating very high chip-to-chip IO and memory bandwidths. Electromechanical complexities have increased non-linearly and continue to have a profound impact on signal integrity at large scale datacenter volumes. New computationally efficient end-to-end link BE simulation and statistical analysis methodologies are developed to predict defect rates based on high volume manufacturing variation of IO interconnects.

**Bio:** Dean Gonzales is an AMD Fellow with three decades of experience working on the design of silicon, advanced packaging technology, and computer systems. His signal integrity focus helps drive AMD pathfinding to improve power, area, and performance of silicon interconnects. Dean brings to this talk a passion for IO electrical standardization and compliant channel design and modeling methodologies.

# Walker Turner

*Nvidia*

High-Speed Interconnects to Enable Chiplet-Based AI Systems



**Abstract:** Chiplet-based architectures enable custom accelerators for deep neural network inference capable of addressing different market needs with one scalable solution. Co-packaging chiplets within a mesh network uses smaller chips with higher yield and reduced design cost to increase system capacity beyond reticle limits. The high-speed wireline links that interconnect these multi-chip systems must provide increasing bandwidth across generations while consuming a fraction of total system power. This comes at a time where we can no longer rely on the consistent transistor-based scaling that historically comes from newer technology nodes. Instead, a co-optimization of the high-speed circuitry, signaling channels, and advanced packaging technology is required to enable future scalability. This includes the use of single-ended signaling to minimize per-pin symbol rates along with other low power circuit techniques.

**Bio:** Walker Turner is a Senior Research Scientist at NVIDIA. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Florida in 2009, 2012, and 2015, respectively. He has been with NVIDIA since 2015, working in the Circuits Research Group. His research focuses on energy-efficient, high-speed signaling for on- and off-chip communication. He also served as a Teaching, Assistant Professor at North Carolina State University from 2019 to 2020 where he instructed an undergraduate micro-electronics course.

# Marko Simičić

*IMEC*

ESD in advanced IC bonding technologies



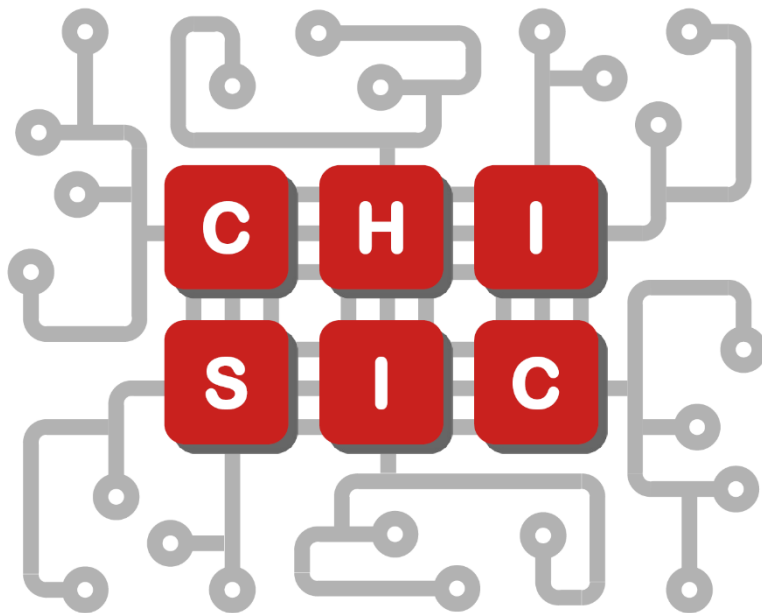
**Abstract:** The integrated circuit technology scaling roadmap is investing heavily on advanced bonding technologies. Bonding multiple chips together into a single system with extremely short interconnects promises to continue increasing integrated-circuits performance regardless of the transistor scaling slowing down. "Chiplets", "2.5D bonding", "3D bonding", "chip-on-wafer", "wafer-on-wafer" and "heterogeneous integration" are some of the terms associated with these advanced bonding technologies. However, system assembly during advanced bonding also raises concerns of electrostatic discharges, or ESD for short. This talk will look into ESD concerns and solutions in advanced bonding technologies from three points of view: ESD protection, ESD testing and ESD prevention, with focus on circuit design.

**Bio:** Marko Simicic received the B.Sc. and M.Sc. degrees in electrical engineering and information technology from the University of Zagreb, Croatia, in 2010 and 2012 respectively. He obtained a PhD degree from the department of electrical engineering ESAT, KU Leuven,

Belgium in 2018. In 2017 he joined the ESD team in imec, Belgium. He is a certified ESD control program manager since 2022. He has authored or co-authored more than 35 papers in international journals and conference proceedings. His current research area includes ESD device and circuit design in advanced semiconductor and 3D/2.5D stacking technologies, novel ESD testing and ESD control process assessment.

Table 1. Workshop agenda

07:00AM	08:00AM	Breakfast	
08:00AM	08:10AM	Workshop Introduction	A. Piovaccari
08:10AM	09:00AM	KEYNOTE: Chiplet-based electronics: evolution or revolution?	A. Sangiovanni-Vincentelli
09:00AM	09:50AM	Advanced Technologies For Next Generation Chiplet Based Data Center CPU	E. Fetzer
09:50AM	10:10AM	Coffee Break	
10:10AM	11:00AM	Harnessing Chiplets for Academic Research	Z. Zhang
11:00AM	11:50AM	Chiplet Reliability and Reliable Use of Chiplet Technology	J. Rupe
11:50AM	12:50PM	Lunch Break	
12:50PM	01:40PM	Chiplet and Heterogeneous Integration with Advanced Packaging Technologies	S. Gao
01:40PM	02:30PM	Scaling Chiplet IO Signal Integrity For The Next Generation Data Center	D. Gonzales
02:30PM	02:50PM	Coffee Break	
02:50PM	03:40PM	High-Speed Interconnects to Enable Chiplet-Based AI Systems	W. Turner
03:40PM	04:30PM	ESD in advanced IC bonding technologies	M. Simičić



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